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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,733	03/15/2004	Sung-Woo Lee	2557-000201/US	9981

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,733	LEE ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim 9 recites the limitation "the mother board heads" in line 3. There is insufficient antecedent basis for this limitation in the claim.

3. For the purpose of Examination and to expedite the prosecution, Examiner assumes that claim 9 reads as follows:

"mechanically binding the mother board to a test head via a load board"

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 8 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeng et al. (US 6097199).

Regarding claims 1 and 8, Jeng et al. (hereafter Jeng) in fig. 2 discloses a coupling arrangement for coupling the same semiconductor device to different models of semiconductor device testers manufactured by different manufacturers, the arrangement comprising:

a mother board [204] electrically compatible with each of respective test heads [206] of the different models of testers [see Abstracts]; and

a device under test (DUT) board [202] connectable between the mother board and a semiconductor device to be tested by one of the different models of tester.

Regarding claims 12-13, Jeng discloses the coupling arrangement of claim 1, further comprising: arranging a first side of the mother board to have terminals [terminals in 316, 318 and 320, see fig. 3B] for test signal paths distributed azimuthally around the center thereof, and arranging a second side of the mother board to have terminals for test signal paths [terminals in 302 for tester, see fig. 3A], respectively, gathered into a relative smaller predetermined area (arcuate in shape).

Regarding claim 14, Jeng discloses the method of claim 8, further comprising electrically connecting test signal paths through the mother board to test signal paths on the DUT board via aligning conductive terminals [terminals in 312, 314 and 304, 302 regions].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-7 and 9-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng as applied to claim 1 and 8 above, and further in view of Applicants admitted prior art fig. 1-4.

Regarding claims 2 and 9, Jeng discloses all the elements except for a load board loading unit to mechanically bind the mother board to any one of the test heads. Applicants admitted prior art (hereafter APA) in fig. 1-4, particularly in fig. 1 discloses a load board loading unit [16] to mechanically bind the mother board [18] to the test head [14]. APA also discloses plurality of mother board i.e. 18A, 18B and 18C in fig. 2-4 respectively for coupling the same semiconductor device under test. Therefore, it would have been obvious to a person having ordinary skill in the art to modify the coupling arrangement of Jeng by adding a load board loading unit as taught by APA, in order to provide mechanical bind of motherboard to a test head.

Regarding claims 3 and 10, Jeng discloses all the elements including different testers to provide electrical signals for testing. However Jeng is silent about the mother board provides signal paths for mixed signals, respectively. APA at paragraph 0009 of the discloser discloses the mother board [18] provides signal paths for mixed signals. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify mother board of Jeng with signal path for mixed signals as taught by APA, in order to test semiconductor device with mixed signals.

Regarding claims 4 and 11, Jeng discloses all the elements except for a plurality of locking units are placed on the mother board for mechanically connecting the DUT board to the mother board. However, at lines 66-67 of column 3 and at lines 1-7 of

column 4, Jeng discloses a mechanically connecting the DUT board 202 to the mother board 204. Therefore, plurality of locking units as claimed is obvious to the Jeng, since it was known in the art that secure connection is needed between DUT board and the mother board during testing to obtain greater accurate result.

Regarding claim 5, Jeng discloses an electrical connection between the respective test head and the semiconductor device is made through a connector [208, see lines 56-58 of column 3] on the mother board.

Regarding claim 6, Jeng discloses all the elements except for the plurality of locking units has the same shape regardless of the particular manufacturer of the tester. It would have been obvious matter of design choice to have the plurality of locking units has the same shape because the plurality of locking units are **on** the motherboard for DUT board and not connected to the tester therefore shape of the plurality of locking units as claimed and the particular manufacturer of the tester are not related. Also, since applicant has not disclosed that having same shape of the plurality of locking units solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with locking units of Jeng.

Regarding claim 7, Jeng discloses all the elements except for the DUT board includes vertical type relays. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use vertical type relays as claimed as switch between different testing (i.e. from digital to analog and vice versa) to test certain characteristic of the semiconductor device (see Small, US 5563509 and Sinsheimer, US 6166553 for use of relay). Also it is a matter of design choice to include vertical type

relays as claimed, since applicant has not disclosed vertical type relays solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with coupling arrangement of Jeng.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paresh Patel
Primary Examiner
Art Unit 2829

June 12, 2005